REMARKS

Applicant concurrently files herewith a petition and fee for a one month extension of time.

Claims 1-18 are presently pending in the application. Claims 1, 3-7, 9, and 12 have been amended to more particularly define the invention. Claims 13-18 have been added to assure Applicant the degree of protection to which his invention entitles him.

Claims 1 and 3 were rejected under 35 U.S.C. §102(a) as being anticipated by Applicant's Admitted Prior Art. Claims 2, 4-5 and 7-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admitted Prior Art in view of Yaegawa, et al., U.S. Patent No. 6,598,137. It is noted that although claim 6 is not explicitly rejected on page 2 or 3 of the Office Action, the applicability of the prior art to claim 6 is discussed on page 5. From this, it is inferred that claim 6 was intended to be rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admitted Prior Art in view of Yaegawa, et al., like claims 2, 4-5, and 7-12. In any event, all the rejections are respectfully traversed.

THE CLAIMED INVENTION

The claimed invention is directed to a microcomputer. In an exemplary embodiment, the microcomputer includes a central processing unit; a data bus electrically connected to the central processing unit; a cache; a command bus electrically connected to the cache and separated from the data bus; and a memory electrically connected to the command bus. The memory stores an interruption handling routine therein. Certain embodiments further include a memory controller which can be connected to an external memory.

Another exemplary embodiment of the microcomputer includes first, second, third, and fourth buses; a central processing unit; a bus controller electrically connected to the central processing unit through the first bus; a command cache electrically connected to the central processing unit through the second bus and to the bus controller through the third bus; and a command memory electrically connected to the second bus through the fourth bus, for storing an interruption handling routine therein. Certain embodiments further include fifth, sixth, and seventh buses; an external memory; and a memory controller electrically connected to the bus controller through the fifth bus, to the command memory through the sixth bus, and to the external memory through the seventh bus.

THE PRIOR ART REFERENCES

Applicant's Admitted Prior Art

Applicant's Admitted Prior Art discloses a microcomputer including a central processing unit; a data bus electrically connected to the central processing unit; a cache; and a command bus electrically connected to the cache and separated from the data bus. The microcomputer does not contain a memory. Instead, an external memory can be connected to the microcomputer.

The Yaegawa Reference

Yaegawa discloses a microcomputer capable of switching memory maps between different memory units.

ARGUMENT

As set forth above, the microcomputer of the present invention includes a central processing unit, a data bus, a command bus which is connected to a cache, and a memory which is connected to the command bus and which stores an interruption handling routine. Consequently, when an interruption handling routine is to be carried out, the central processing unit can swiftly get the interruption handling routine from the memory through the command bus. Furthermore, since the interruption handling routine is not stored in the cache, delays which might be caused by cache mishitting are avoided.

Because the microcomputer in accordance with the present invention includes the command bus through which a command is transferred from the command memory and which is independent of other buses, particularly the data bus, the speed and efficiency of interruption handling is enhanced.

In contrast, in Applicant's Admitted Prior Art, as illustrated in Figure 1, command bus 45 is not connected to external memory 51. Therefore, Applicant's Admitted Prior Art does not provide the advantages obtained by the claimed invention. Thus, Applicant's Admitted Prior Art does not anticipate the claimed invention.

Additionally, the Office Action contends that Applicant's Admitted Prior Art describes a microcomputer comprising a cache, a central processing unit, and a memory, and contends that component 51 in Figure 1 of the present application is the memory of this prior art microcomputer, but this is incorrect.

The microcomputer of Applicant's Admitted Prior Art is depicted in Figure 1 and

described on page 1, lines 12-17 of the specification. As there described, the microcomputer 41 includes only a central processing unit 42, a bus controller 44, a command cache 47, and a memory controller 49. The specification continues on page 1, in lines 18 and 19 to state that the memory controller 49 is electrically connected to an external memory 51 through an external bus 50. Thus, microcomputer 41 is connected to external memory 51; microcomputer 41 does not include memory 51. Memory 51 is a separate device which must be connected to external bus 50 if memory 51 is going to be used in conjunction with microcomputer 41.

The claimed microcomputer includes a memory. This is command memory 12 depicted in Figure 2. An external memory 51 can be connected to the claimed microcomputer. Since, the microcomputer of Applicant's Admitted Prior Art does not include a memory, Applicant's Admitted Prior Art does not anticipate the invention of claims 1 and 3.

Yaegawa does not add that which distinguishes the claimed invention from Applicant's Admitted Prior Art. Yaegawa's Figures 2 and 6 show that his central processing unit 2, random access memory 3, boot read only memory 5, and flash memory 4 or nonvolatile memory 14 are electrically connected to one another through buses. However Yaegawa's microcomputer does not include a cache or a data bus and a command bus that are independent of, or separated from each other. Thus, Yaegawa, combined with Applicant's Admitted Prior Art Yaegawa does not make obvious the subject matter of claims 2 and 4-12, or of claims 1 and 3.

If Applicant's Admitted Prior Art were combined with Yaegawa, the resulting

structure would have the internal bus 48, depicted in Figure 1 of the present application, electrically connected to Yaegawa's random access memory 3, boot read only memory 5 and flash memory 4 or nonvolatile memory 14. This combination would not anticipate or make obvious the claimed invention.

It is accordingly submitted that the claims distinguish patentably over Applicant's Admitted Prior Art, whether considered alone or in combination with Yaegawa.

FORMAL MATTERS

The Office Action objects to page 9, line 19 of the specification as showing a memory address range of " '0000000H' to '0100000H' " which overlaps the memory address range of " '0100000H' and later." This has been corrected, not only at page 9, line 19, but also on pages 10 and 11.

The Office Action does not indicate that the formal drawings are acceptable. An indication that the formal drawings are acceptable is respectfully requested.

CONCLUSION

In view of the foregoing, Applicant submits that claims 1-18, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number

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listed below to discuss any other changes deemed necessary for allowance in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. The Commissioner is authorized to charge any deficiency in fees, including extension of time fees, or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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